MICROPROCESSOR WITH PACKING OPERATION OF COMPOSITE OPERANDS

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Abstract of **WO9617291**

A processor includes a first register (209) for storing a first packed data, a decoder (202), and a functional unit (203). The decoder has a control signal input (207) for receiving a first control signal and a second control signal. The first control signal is for indicating a pack operation, and the second control signal is for indicating an unpack operation. The functional unit is coupled to the decoder (202) and the register (209). The functional unit performs the pack operation and the unpack operation using the first packed data as well as move operation.